AMENDMENTS TO THE SPECIFICATION

Substitute the following paragraph at Page 14, lines 22-36:

Within delay lock loop 600, reference clock signal REF_CLK is delayed by delay line 610 to generate delayed clock signal D_CLK. Delayed clock signal D_CLK is delayed from clock signal REF_CLK by a propagation delay D in delay line 610. One embodiment of delay lock loop 600 uses an adjustable delay line described in U.S. Patent ~~Application Serial No. 09/102,704 (Attorney Docket No. X-440)~~No. 6,400,735 B1 issued on June 4, 2002, entitled "Glitchless Delay Line Using Gray Code Multiplexer" by Andrew K. Percey, which is incorporated herein by reference. However, other adjustable delay lines can also be used with delay lock loop 600. Delayed clock signal D_CLK is provided to an input terminal of a clock phase shifter 650 and to an input terminal of an output generator 640. Delayed clock signal D_CLK is also provided to digital frequency synthesizer 320 as synchronizing clock signal SYNCH_CLK.